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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	10686	(SUNDARAVEL near VALE) (PAUL near BENJAMIN) switchboard	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 12:35
L12	422	11 and (gps (global adj position$3) ((geograph$6 physical$3) adj2 (point plac$3 position$4 locat$4 situat$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 12:36
L13	24	12 and ((binary bitwise or bit byte bytewise) near2 (compar$5 match$5 check$3 examin$6))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 12:36
L14	11	13 and ((certain$4 or uncertain$4 approximat$5 or accura$6 precis$5 exact$4 correct$5) near2 (binary or bit or bitwise or digit$4 byte bytewise))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 12:48

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L23	9	(binary and bitwise and (compar$5 match$5 check$3 examin$6) and (geograph$7 physica$4 loca$7 position$3 situat$4 coordinat$5) and (information data featur$3) and (certain$4 or uncertain$4 approximat$5 accura$6 precis$5 exact$4 correct$5) and (associat$4 relat$3 connect$3 assign$4 appoint$4)).CLM.	US-PGPUB	OR	ON	2006/06/07 14:56

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	200	380/258	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 12:13
L9	96	8 and (gps (global adj position$3) ((geograph$6 physical$3) adj2 (point plac$3 position$4 locat$4 situat$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 12:14
L10	5	9 and ((binary bitwise or bit byte bytewise) near2 (compar$5 match$5 check$3 examin$6))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 12:15

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1 HAVEGE: A user-level software heuristic for generating empirically strong random numbers
André Seznec, Nicolas Sendrier
October 2003 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 13 Issue 4
Publisher: ACM Press
Full text available: 🔺 pdf(122.28 KB)   Additional Information: full citation, abstract, references, index terms

Random numbers with high cryptographic quality are needed to enhance the security of cryptography applications. Software heuristics for generating empirically strong random number sequences rely on entropy gathering by measuring unpredictable external events. These generators only deliver a few bits per event. This limits them to being used as seeds for pseudorandom generators.General-purpose processors feature a large number of hardware mechanisms that aim to improve performance: caches, branch ...

Keywords: Cryptography, hardware clock counters, random number generation, superscalar processor

2 Modeling for text compression
Timothy Bell, Ian H. Witten, John G. Cleary
December 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 4
Publisher: ACM Press
Full text available: 🔺 pdf(3.54 MB)   Additional Information: full citation, abstract, references, citings, index terms, review

The best schemes for text compression use large models to help them predict which characters will come next. The actual next characters are coded with respect to the prediction, resulting in compression of information. Models are best formed adaptively, based on the text seen so far. This paper surveys successful strategies for adaptive modeling that are suitable for use in practical text compression systems. The strategies fall into three main classes: finite-context modeling, i ...

3 Emerging applications: Obfuscation of executable code to improve resistance to static disassembly
Cullen Linn, Saumya Debray
October 2003 **Proceedings of the 10th ACM conference on Computer and**

communications security

Publisher: ACM Press

Full text available: 📄 pdf(155.75 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

A great deal of software is distributed in the form of executable code. The ability to reverse engineer such executables can create opportunities for theft of intellectual property via software piracy, as well as security breaches by allowing attackers to discover vulnerabilities in an application. The process of reverse engineering an executable program typically begins with disassembly, which translates machine code to assembly code. This is then followed by various decompilation steps that ai ...

Keywords: code obfuscation, disassembly

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4 <u>Optimal VLSI circuits for sorting</u>   ☐

Richard Cole, Alan Siegel

October 1988 **Journal of the ACM (JACM)**, Volume 35 Issue 4

Publisher: ACM Press

Full text available: 📄 pdf(2.81 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

This work describes a large number of constructions for sorting N integers in the range [0, M - 1], for $N \leq M \leq N2$, for the standard VLSI bit model. Among other results, we attain: VLSI sorter constructions that are within a constant factor of optimal size, for all M and almost all running times T. a ...

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5 <u>Level set and PDE methods for computer graphics</u>   ☐

David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker

August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**

Publisher: ACM Press

Full text available: 📄 pdf(17.07 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

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6 <u>GERTIS: a Dempster-Shafer approach to diagnosing hierarchical hypotheses</u>   ☐

John Yen

May 1989 **Communications of the ACM**, Volume 32 Issue 5

Publisher: ACM Press

Full text available: 📄 pdf(1.40 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>, <u>review</u>

Gertis—a prototype expert system—not only demonstrates the feasibility of applying the Dempster-Shafer-based reasoning model to diagnosing hierarchically related hypotheses, but also suggests ways to generate better explanations by using knowledge about the structure of the hypothesis space and knowledge about the intended effects of the rules.

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7 <u>Responses to NIST's proposal</u>   ☐

Ronald L. Rivest, Martin E. Hellman, John C. Anderson, John W. Lyons

July 1992 **Communications of the ACM**, Volume 35 Issue 7

Publisher: ACM Press

Full text available: 🔲 pdf(8.06 MB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

8 <u>Estimation of distribution algorithms: On the convergence of an estimation of distribution algorithm based on linkage discovery and factorization</u>
Alden H. Wright, Sandeep Pulavarty
June 2005 **Proceedings of the 2005 conference on Genetic and evolutionary computation GECCO '05**
Publisher: ACM Press
Full text available: 🔲 pdf(146.80 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

Estimation of distribution algorithms construct an explicit model of the problem to be solved, and then use this model to guide the search for good solutions. For an important class of fitness functions, namely those with k-bounded epistasis, it is possible to construct a complete explicit representation of the fitness function by sampling the fitness function. A very natural model of the problem to be solved is the Boltzmann distribution of the fitness function, which is an exponential o ...

Keywords: Boltzmann distribution, estimation of distribution algorithms, evolutionary computation, factorization, genetic algorithms

9 <u>HYDRO: a heterogeneous distributed database system</u>
William Perrizo, Joseph Rajkumar, Prabhu Ram
April 1991 **ACM SIGMOD Record , Proceedings of the 1991 ACM SIGMOD international conference on Management of data SIGMOD '91**, Volume 20 Issue 2
Publisher: ACM Press
Full text available: 🔲 pdf(810.64 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

10 <u>Trajectory sampling for direct traffic observation</u>
N. G. Duffield, Matthias Grossglauser
June 2001 **IEEE/ACM Transactions on Networking (TON)**, Volume 9 Issue 3
Publisher: IEEE Press
Full text available: 🔲 pdf(251.55 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Traffic measurement is a critical component for the control and engine ering of communication networks. We argue that traffic measurement should make it possible to obtain the spatial flow of traffic through the domain, i.e., the paths followed by packets between any ingress and egress point of the domain. Most resource allocation and capacity planning tasks can benefit from such information. Also, traffic measurements should be obtained without a routing model and without knowledge of netw ...

Keywords: Hash functions, Internet traffic measurement, packet sampling, traffic engineering

11 <u>Power minimization in IC design: principles and applications</u>
Massoud Pedram
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1
Publisher: ACM Press
Full text available: 🔲 pdf(550.02 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

12 Trajectory sampling for direct traffic observation

N. G. Duffield, M. Grossglauser

August 2000 **ACM SIGCOMM Computer Communication Review, Proceedings of the conference on Applications, Technologies, Architectures, and Protocols for Computer Communication SIGCOMM '00**, Volume 30 Issue 4

Publisher: ACM Press

Full text available: pdf(421.07 KB)   Additional Information: full citation, abstract, references, citings, index terms

Traffic measurement is a critical component for the control and engineering of communication networks. We argue that traffic measurement should make it possible to obtain the spatial flow of traffic through the domain, i.e., the paths followed by packets between any ingress and egress point of the domain. Most resource allocation and capacity planning tasks can benefit from such information. Also, traffic measurements should be obtained without a routing model and without knowledge of netwo ...

13 Data and memory optimization techniques for embedded systems

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg

April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2
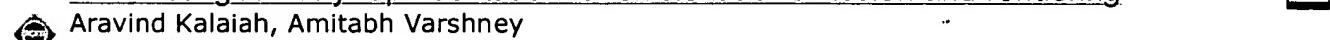
Publisher: ACM Press

Full text available: pdf(339.91 KB)   Additional Information: full citation, abstract, references, citings, index terms

We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transoformations. We next cover a broad spectrum of optimizati ...

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey

14 Statistical geometry representation for efficient transmission and rendering

Aravind Kalaiah, Amitabh Varshney

April 2005 **ACM Transactions on Graphics (TOG)**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: pdf(16.46 MB)   Additional Information: full citation, abstract, references, index terms

Traditional geometry representations have focused on representing the details of the geometry in a deterministic fashion. In this article we propose a statistical representation of the geometry that leverages local coherence for very large datasets. We show how the statistical analysis of a densely sampled point model can be used to improve the geometry bandwidth bottleneck, both on the system bus and over the network as well as for randomized rendering, without sacrificing visual realism. Our s ...

Keywords: Point-based rendering, network graphics, principal component analysis, programmable GPU, progressive transmission, quasi-random numbers, view-dependent rendering

15 Strength of two data encryption standard implementations under timing attacks

Alejandro Hevia, Marcos Kiwi
November 1999 **ACM Transactions on Information and System Security (TISSEC)**,
Volume 2 Issue 4
Publisher: ACM Press

Full text available: pdf(183.73 KB)   Additional Information: full citation, abstract, references, citings, index terms, review

We study the vulnerability of two implementations of the Data Encryption Standard (DES) cryptosystem under a timing attack. A timing attack is a method, recently proposed by Paul Kocher, that is designed to break cryptographic systems. It exploits the engineering aspects involved in the implementation of cryptosystems and might succeed even against cryptosys-tems that remain impervious to sophisticated cryptanalytic techniques. A timing attack is, essentially, a way of obtaining some users ...

Keywords: cryptanalysis, cryptography, data encryption standard, timing attack

16 Practical advances in asynchronous design and in asynchronous/synchronous interfaces

Erik Brunvand, Steven Nowick, Kenneth Yun
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(155.17 KB)   Additional Information: full citation, references, citings, index terms

17 Recursive array layouts and fast parallel matrix multiplication

Siddhartha Chatterjee, Alvin R. Lebeck, Praveen K. Patnala, Mithuna Thottethodi
June 1999 **Proceedings of the eleventh annual ACM symposium on Parallel algorithms and architectures**
Publisher: ACM Press
Full text available: pdf(1.28 MB)   Additional Information: full citation, references, citings, index terms

18 Efficient exact arithmetic for computational geometry

Steven Fortune, Christopher J. Van Wyk
July 1993 **Proceedings of the ninth annual symposium on Computational geometry**
Publisher: ACM Press

Full text available: pdf(982.06 KB)   Additional Information: full citation, abstract, references, citings, index terms

We experiment with exact integer arithmetic to implement primitives for geometric algorithms. Naive use of exact arithmetic—either modular or multiprecision integer—

increases execution time dramatically over the use of floating-point arithmetic. By combining tuned multiprecision integer arithmetic and a floating-point filter based on interval analysis, we can obtain the effect of exact integer arithmetic at a cost close to that of floating-point arithmetic. We describe an experi ...

Results 1 - 18 of 18

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